

FIG. 1

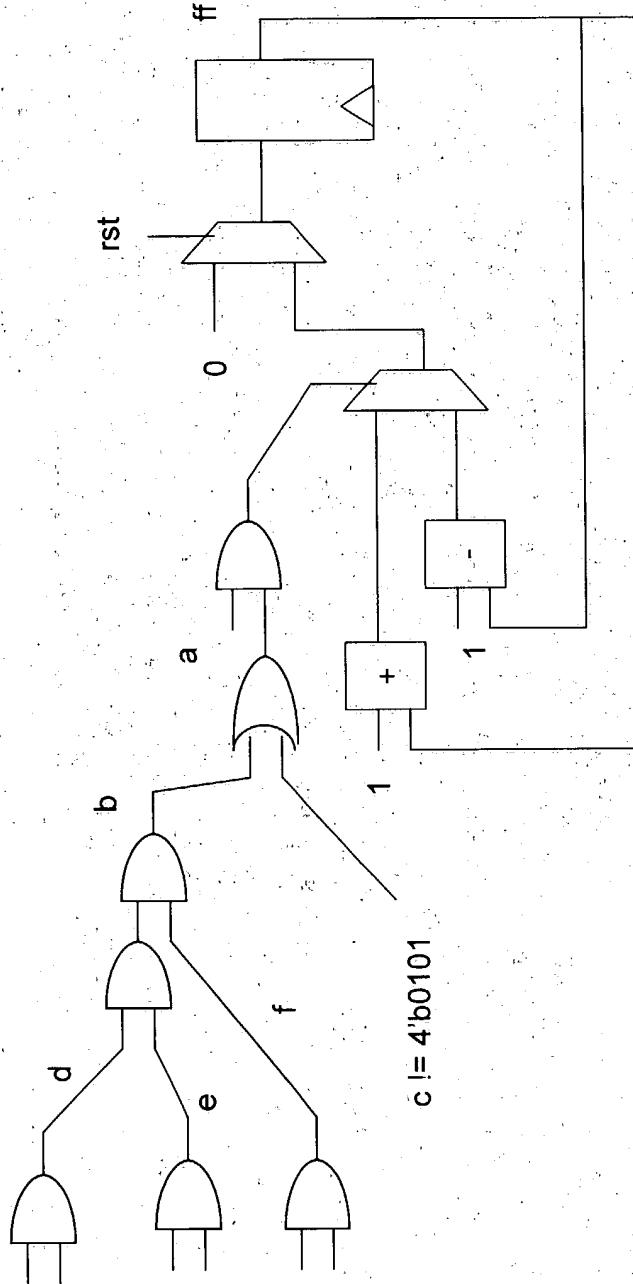


FIG. 2

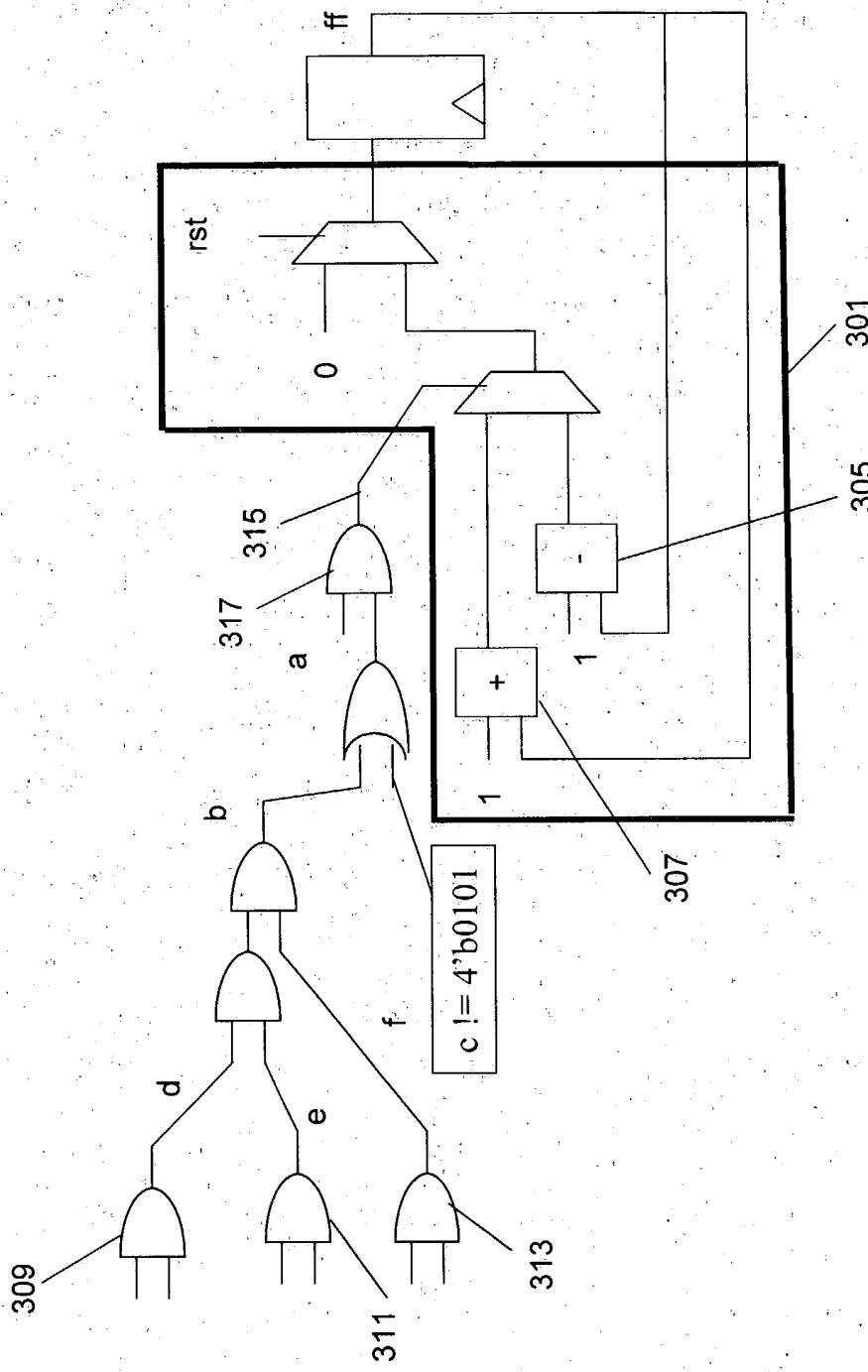


FIG. 3

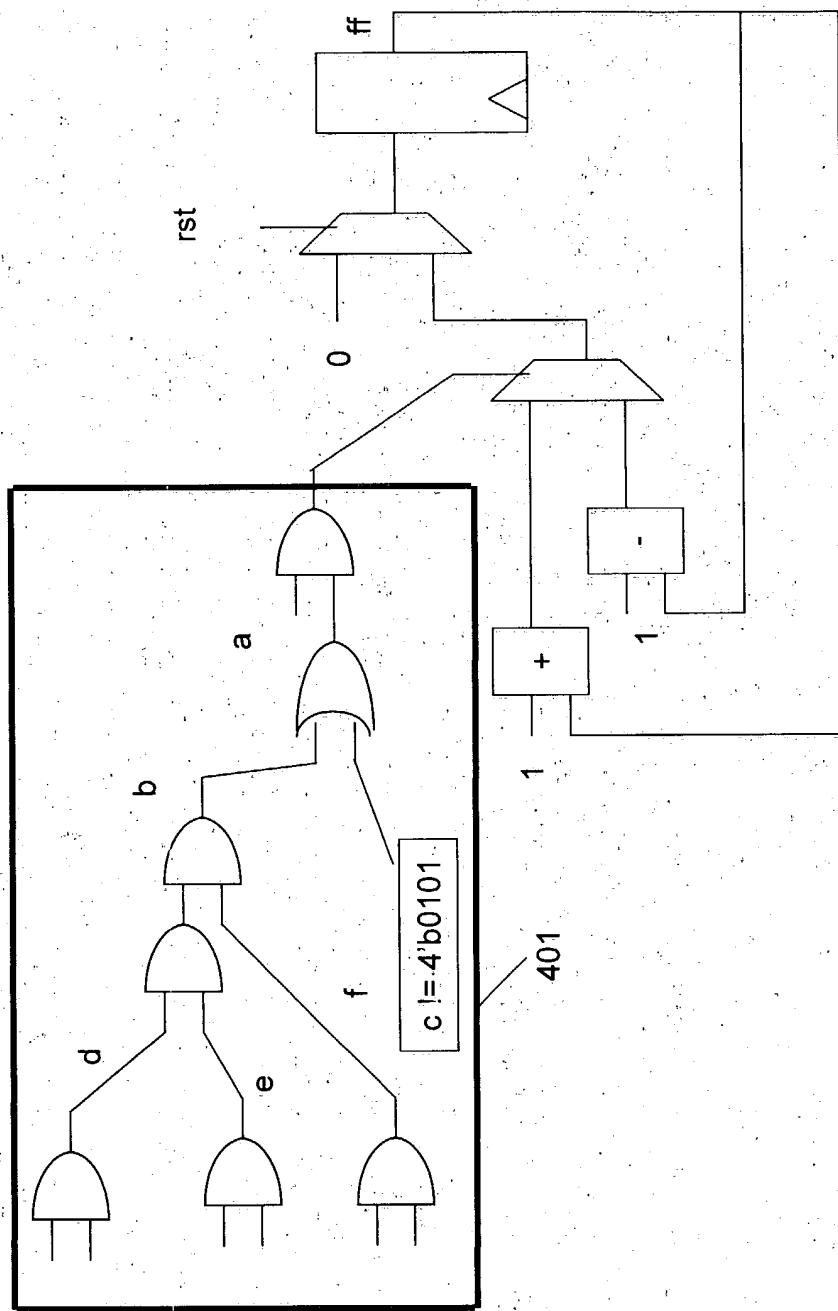


FIG. 4

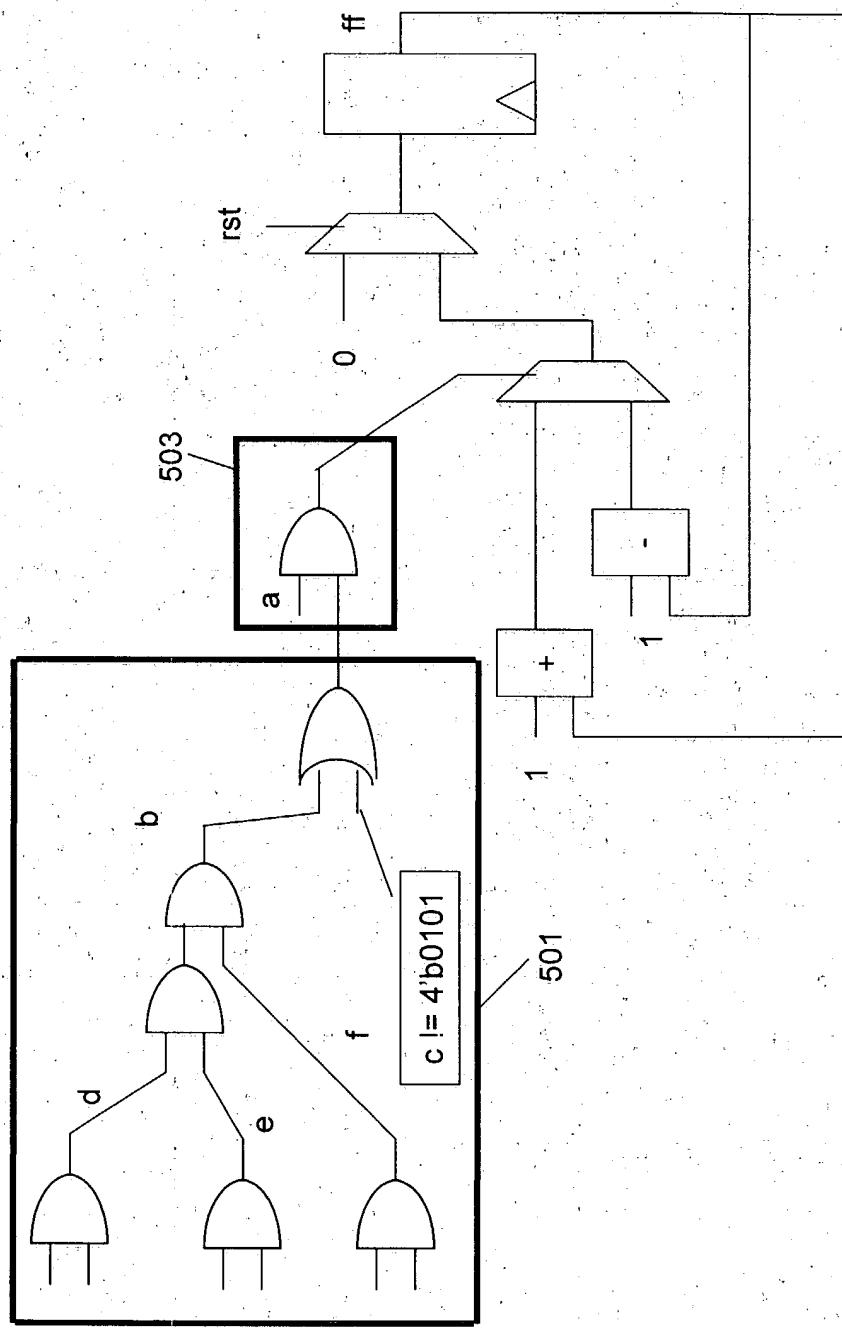


FIG. 5

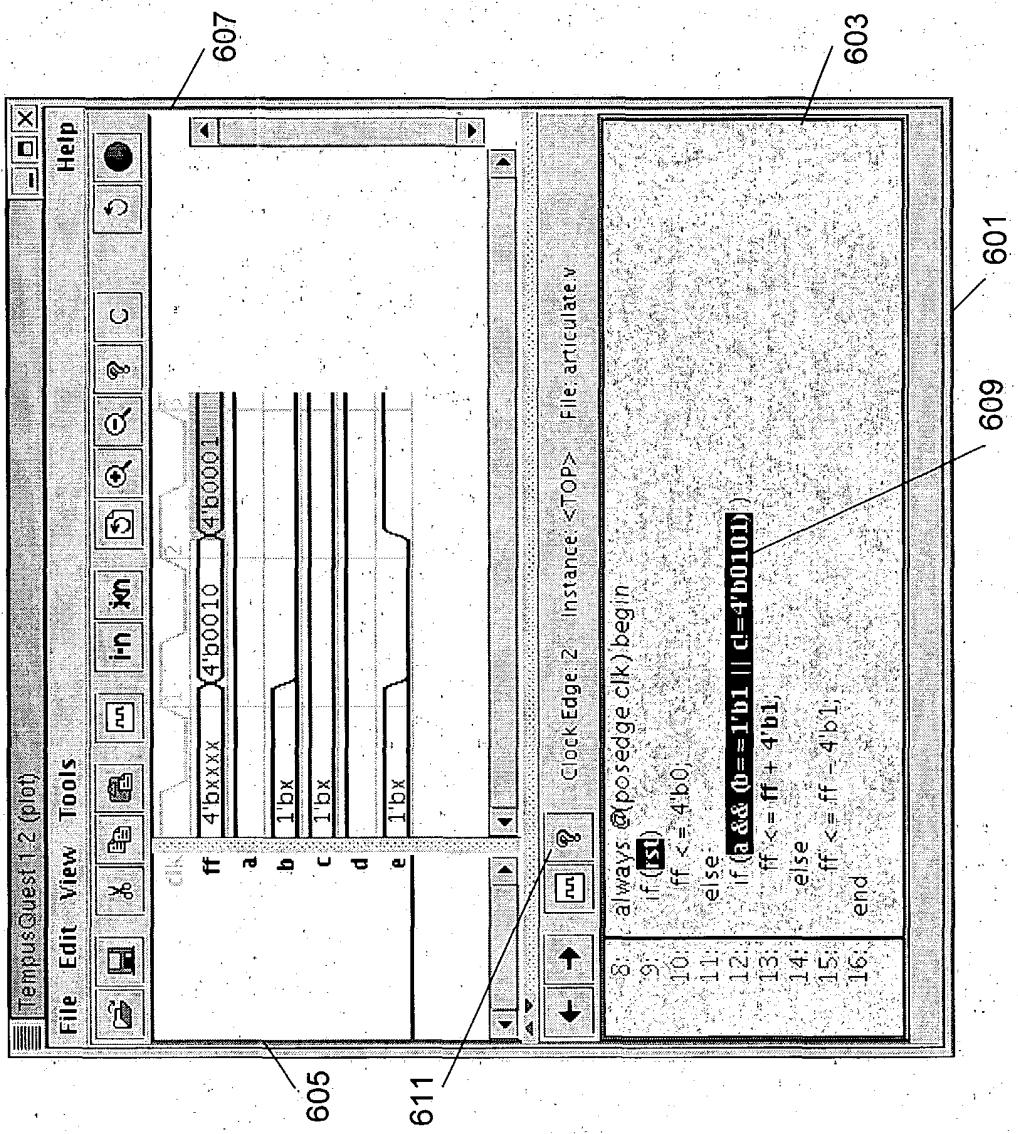


FIG. 6

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FIG. 7

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The screenshot shows the TempusQuest 1.2 software interface. On the left is a logic simulation window with waveforms for signals ff, a, b, c, d, and e. The signal ff starts at 4'b0000, then goes to 4'b0001, and finally to 4'b0000. Signals a, b, c, d, and e are all 1'bX. On the right is a VHDL code editor with the following code:

```

8  always @ (posedge clk) begin
9    if ((st)
10      ff <= 4'b0,
11    else
12      if (d & (b = 1'b1 || c = 4'b101))
13        ff <= ff + 4'b1;
14      else
15        ff <= ff - 4'b1;
16    end

```

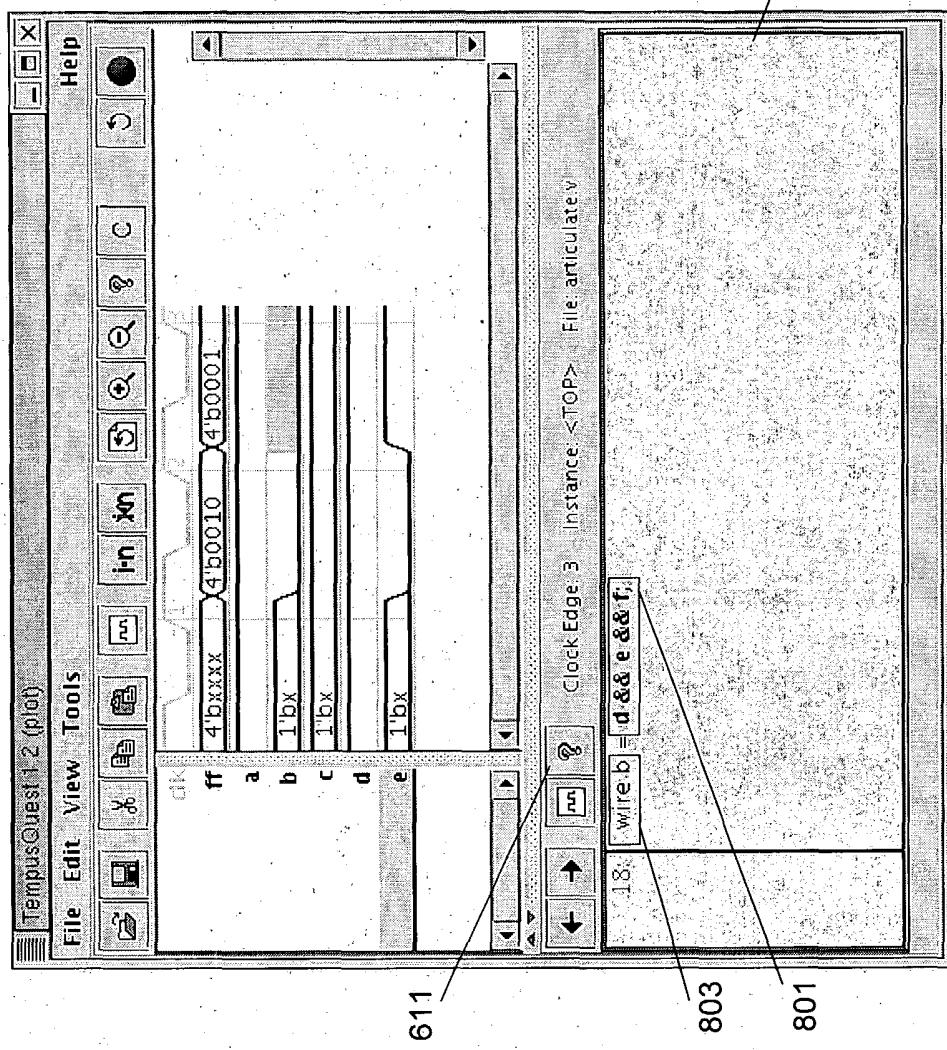


FIG. 8

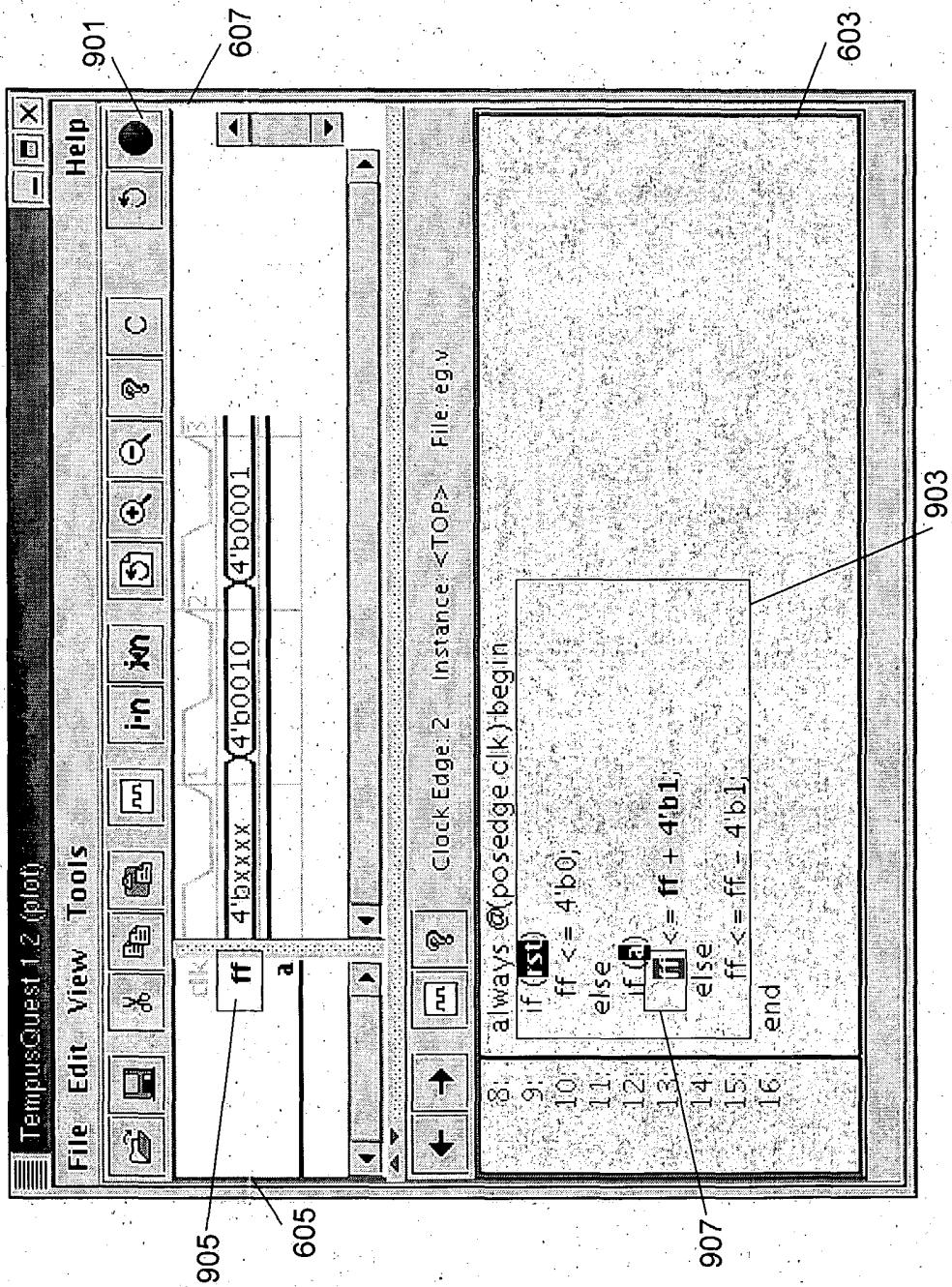


FIG. 9

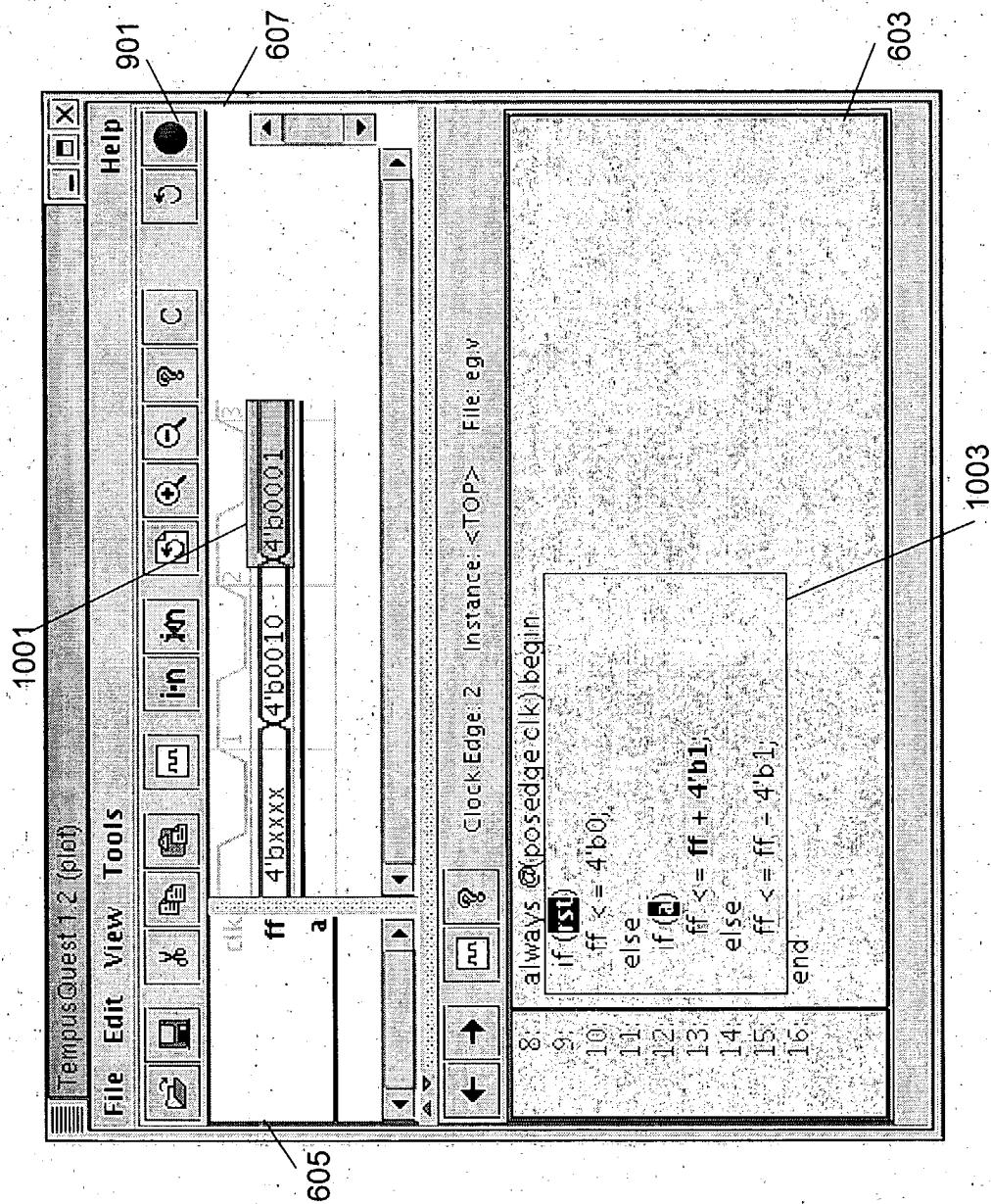


FIG. 10

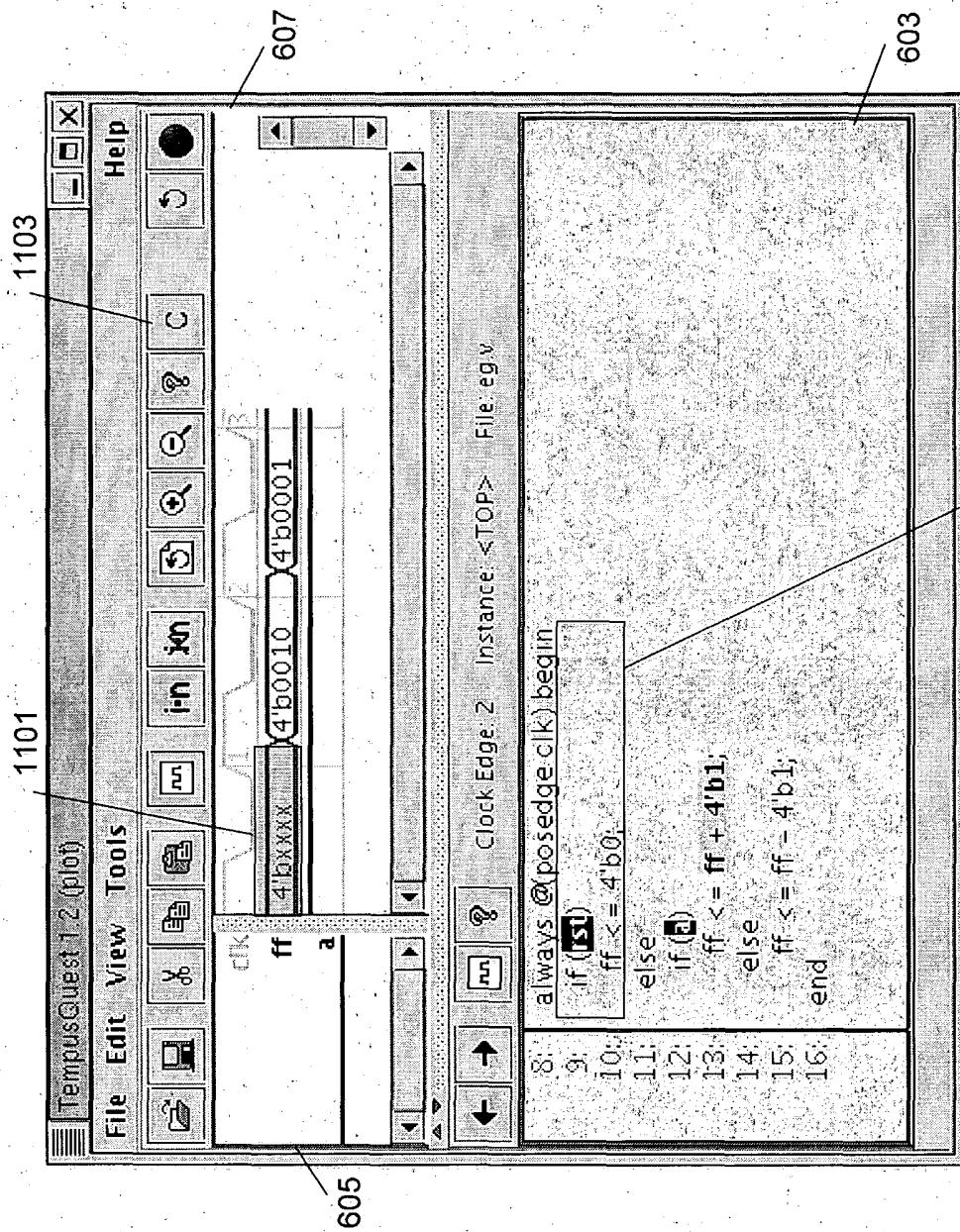


FIG. 11

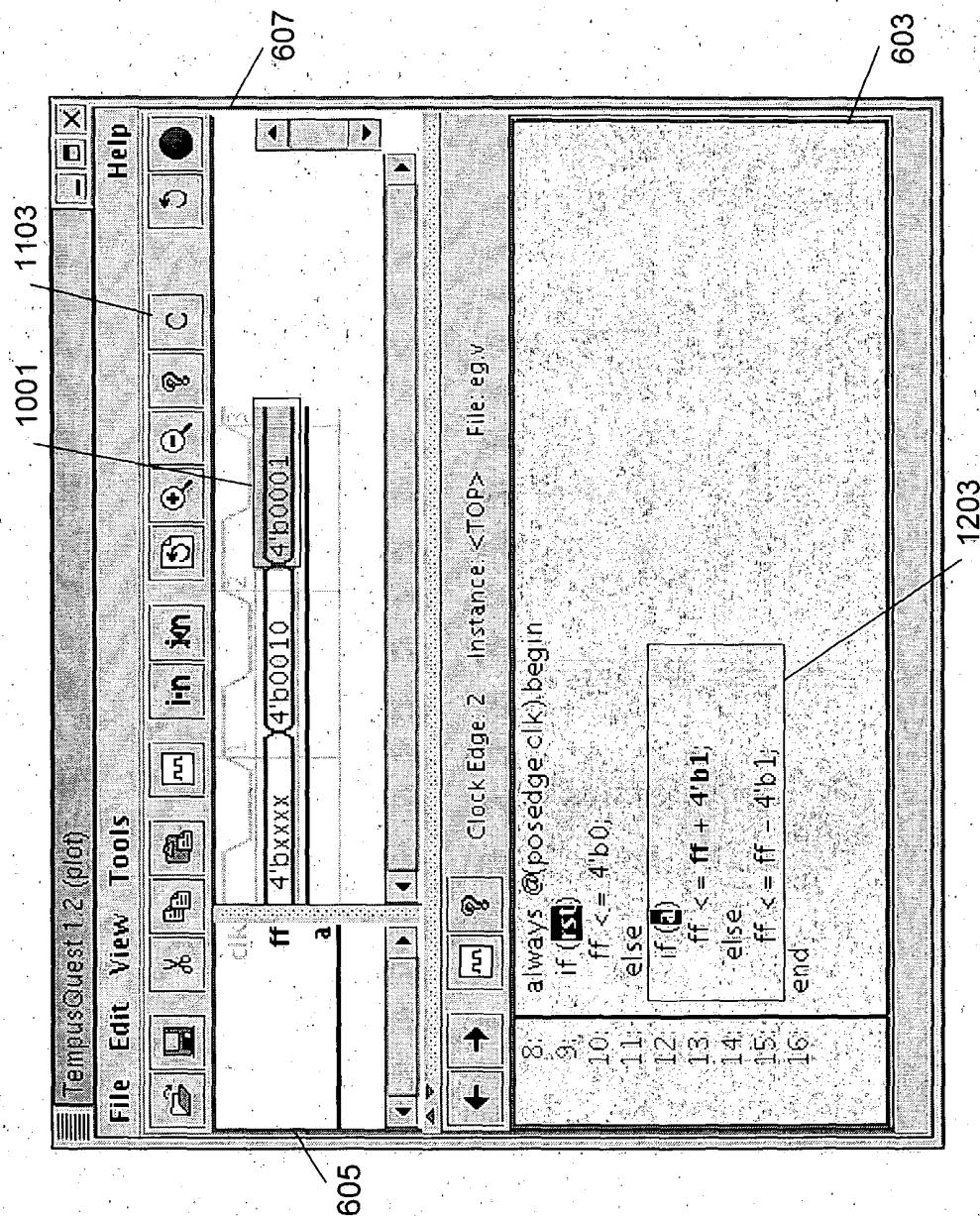


FIG. 12

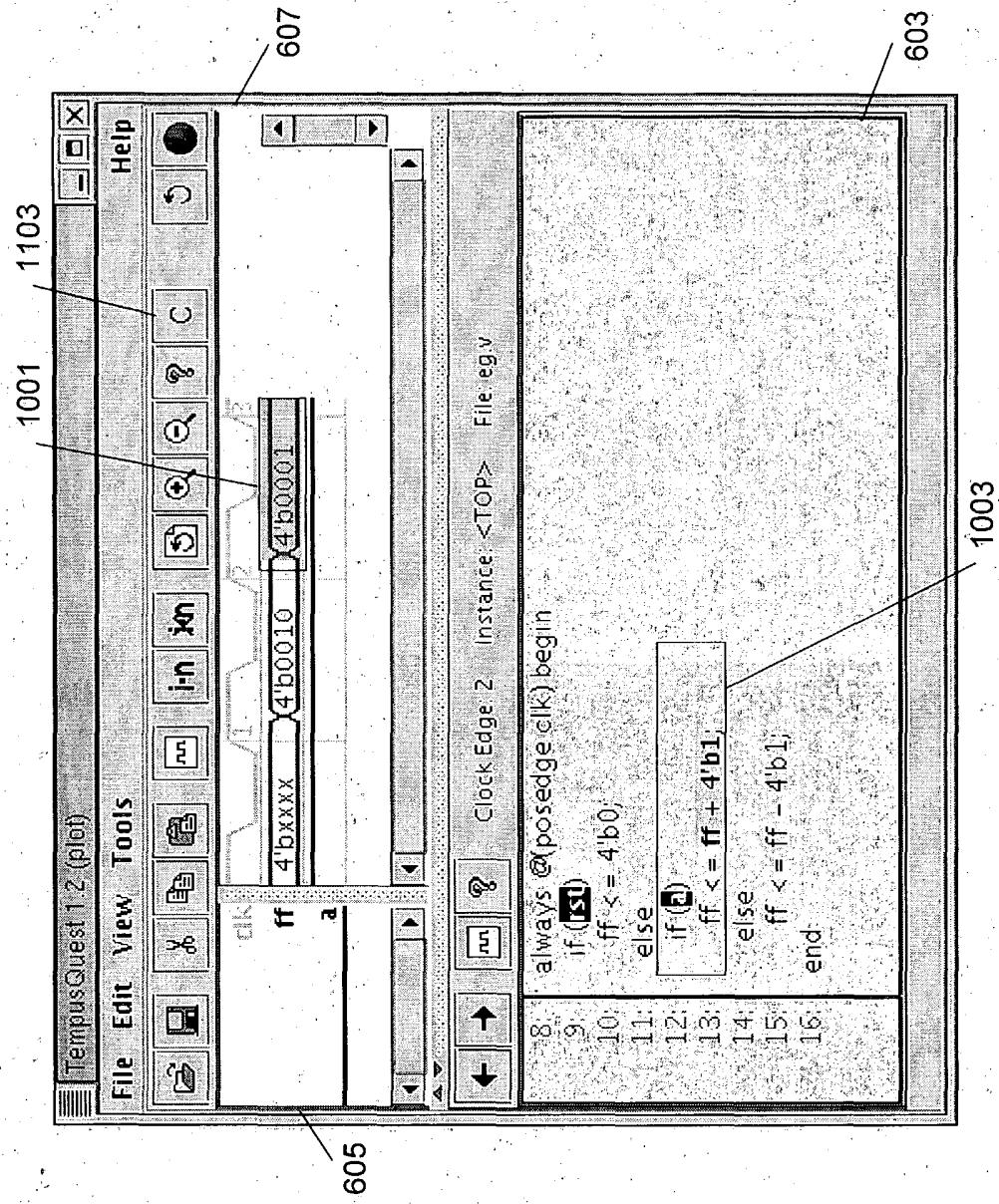


FIG. 13

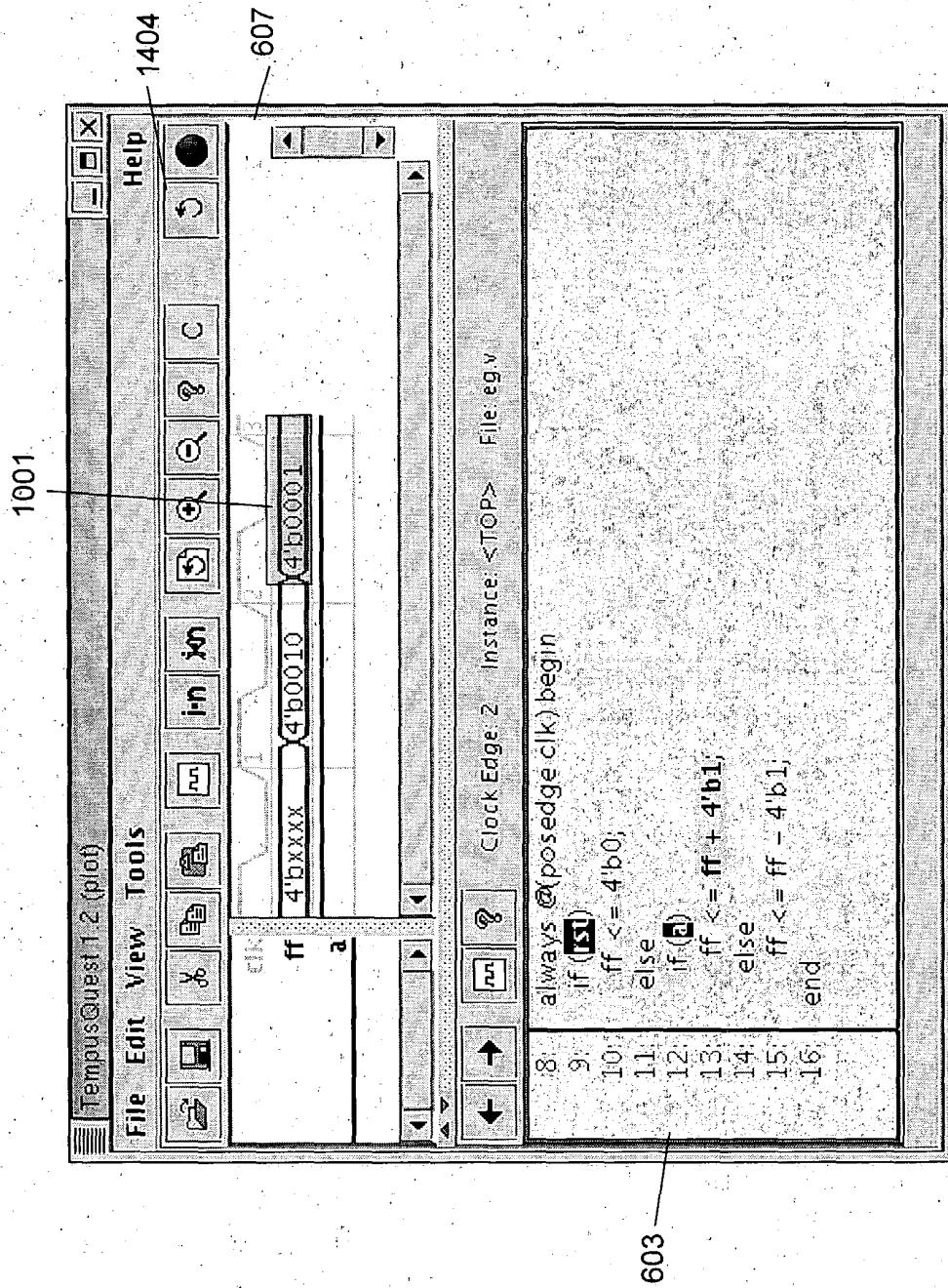


FIG. 14

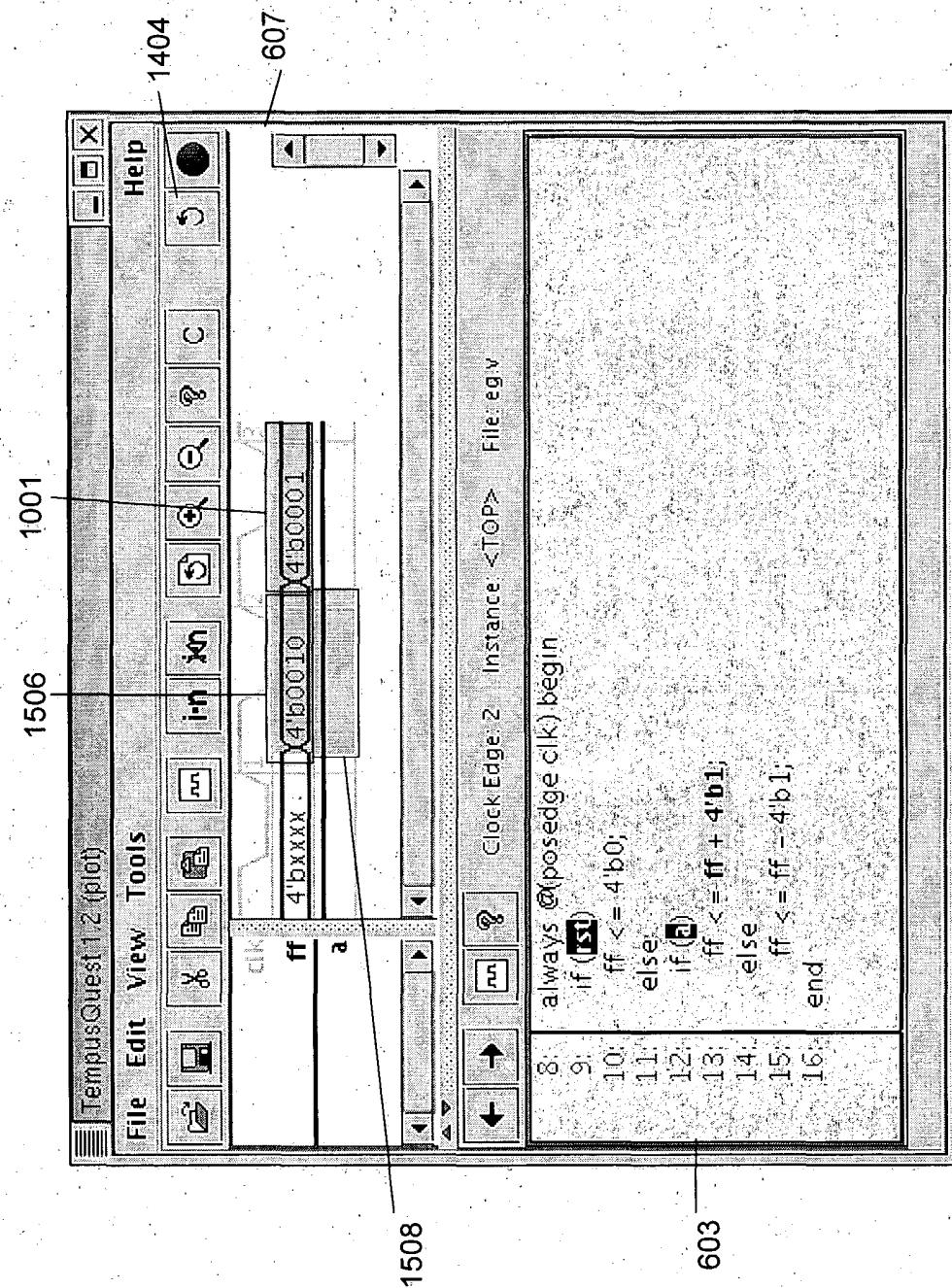


FIG. 15

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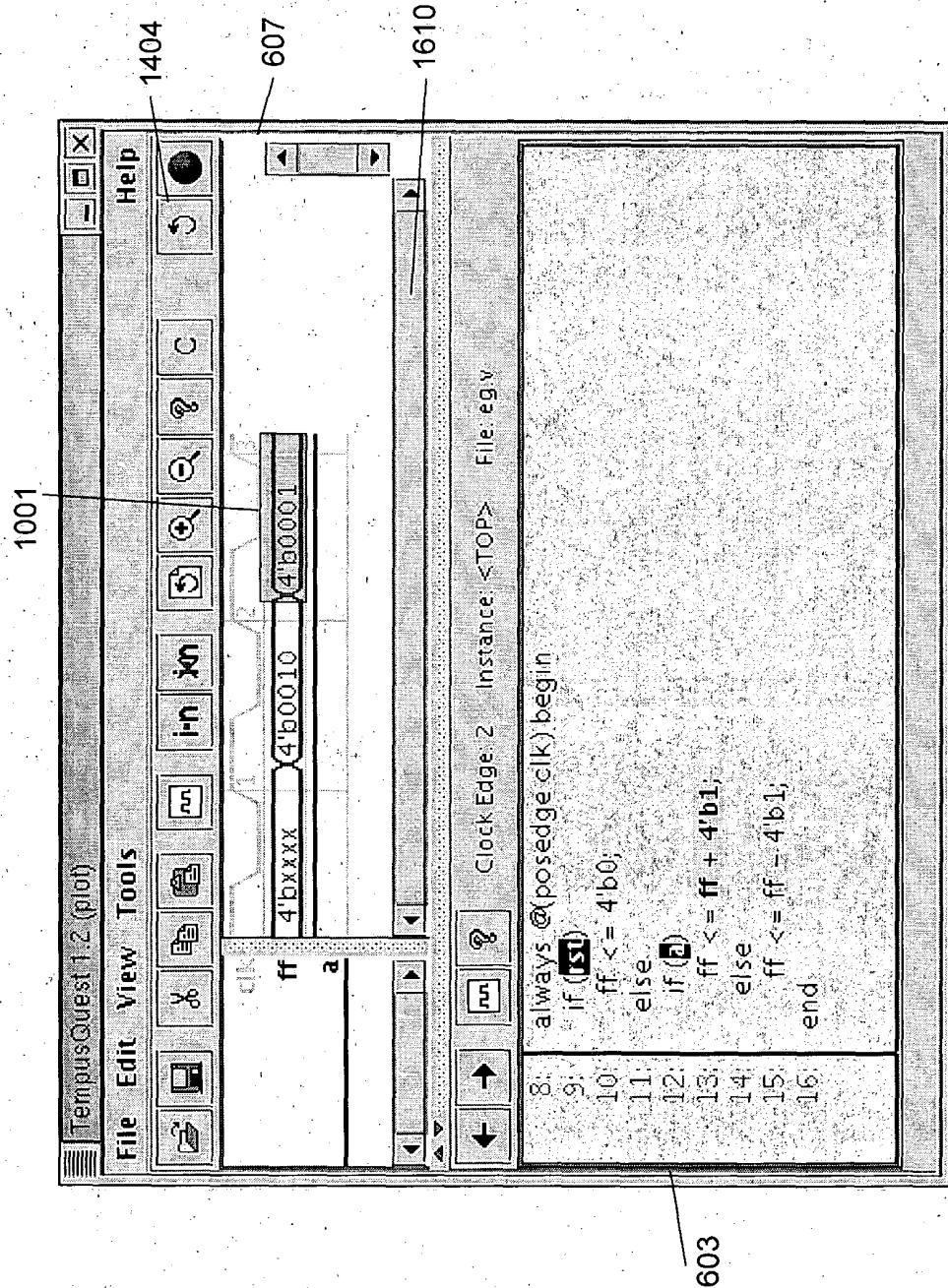


FIG. 16